The Pattern Metrology Puzzle:
Piecing Together a Control Strategy for 65-nm and Beyond

September 29, 2005

Kevin Lensing
Advanced Micro Devices

Agenda

- Introduction
- Overview of pattern metrology
  - Pattern fidelity metrology
  - Pattern placement metrology
- Trends & Conclusions

Metrology "facts" you may have heard…

Overlay metrology is not a big concern

Scatterometry is not a viable production technology

You can't do wafer-level control without integrated metrology

Scatterometry will replace CD-SEM technology

CD-SEM technology has reached its physical limit

CD-SEM can't meet precision requirements for ~~180 nm~~

~~130-nm~~

90-nm

Integrated metrology is an "all or nothing" proposition

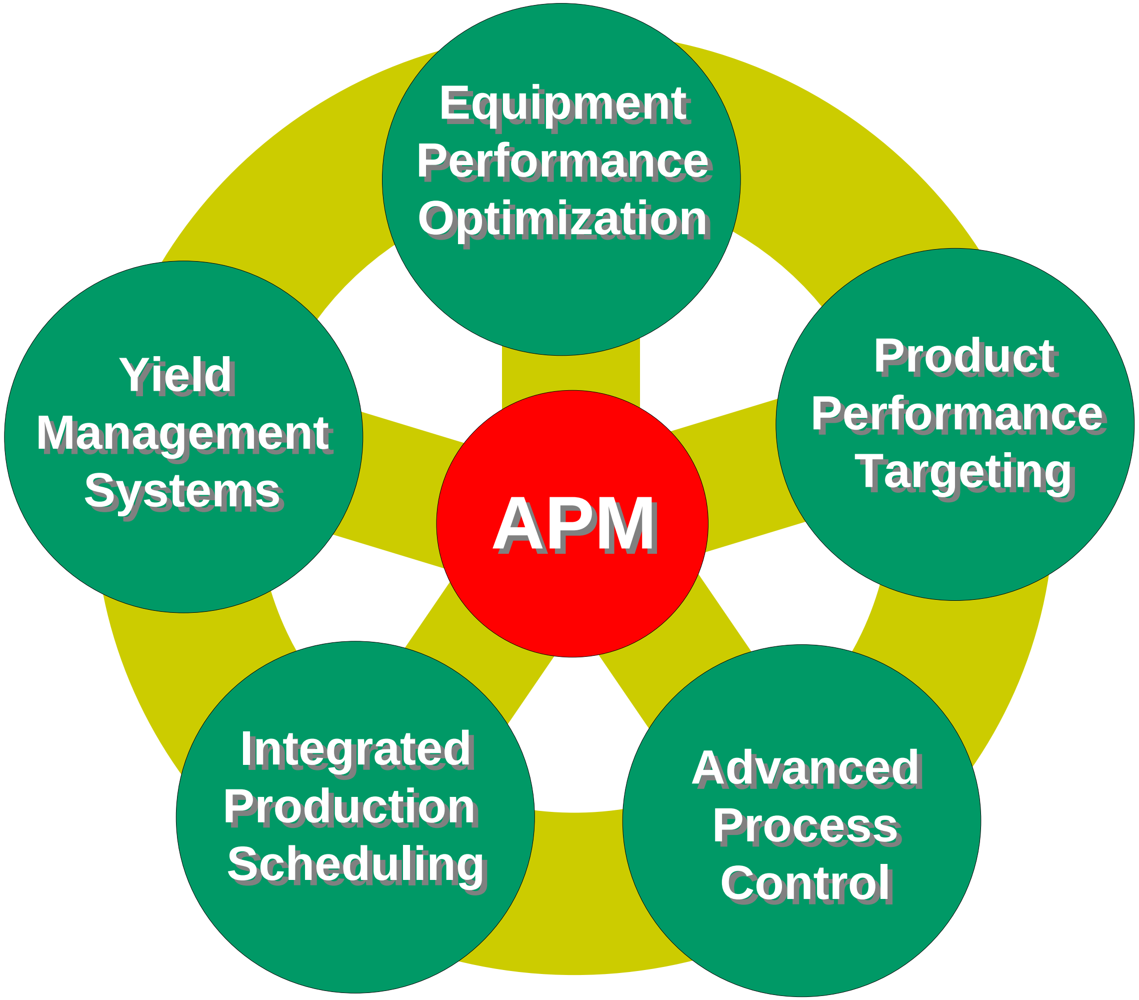
What should we believe?

- Pattern metrology is evolutionary, not revolutionary
  - The CD-SEM did not die, ***but*** the ROI is becoming more difficult and the technical challenges are mounting
  - Scatterometry will not fully replace the CD-SEM, ***but*** it is a growing part of the pattern metrology mix
  - Companies will not “make the switch” from stand-alone to integrated metrology, ***but*** the case for IM will expand with time
  - Change in overlay metrology is just beginning, and we are likely to see the same evolutionary trends

- The challenge for chipmakers is to find the right mix of technologies to enable their manufacturing vision

So what is AMD’s Vision?

Automated Precision Manufacturing (APM)



Highly Automated and Integrated *Decision Making*

+

Non-Stop Cycle of Technology Improvement

+

Maximum Efficiency in Material Handling

Evolution of Automated Control

Evolution of Control

Stability

- Automated SPC and Data Collection
- Manual Process Control

Controllability

- Automated Closed-Loop Process Control
- MISO Fault Detection Capability
- Framework Based Control Solutions

Predictability

- Supervisory Control Applications
- Advanced Measurement Technology
- Automated Controller Monitoring
- Integration of APC and other Factory Systems

Optimization

- Holistic, automated decision making.
- Factory Wide Control
- Large-Scale factory systems integration (APC,IPS,YMS)
- Real Time Factory Optimization
- **Advanced Metrology with Optimized Measurement Plans**

Late 80's | Late 90's | 2000 & beyond

← Control Evolution →

AMD

ITRS Litho Roadmap

Technology Node	2004	2007	2010	2013	2016	2018
Technology Node	90 nm	65 nm	45 nm	32 nm	22 nm	18nm
MPU ½ Pitch (nm)	107	76	54	38	25	21
MPU Printed Gate Length (nm)	53	35	25	18	13	10
MPU Physical Gate Length (nm)	37	25	18	13	9	7
Lithography Metrology						
Printed Gate CD Control (nm) Allowed Litho Variance = 4/5 Total Variance of physical gate length	3.3	2.2	1.6	1.2	0.8	0.6
Wafer CD Tool 3σ Precision P/T=0.2 for Printed and Physical Isolated Lines	0.7	0.4	0.3	0.2	0.2	0.1
Wafer CD metrology tool precision (nm) * (P/T=.2 for dense lines**)	2.2	1.6	1.1	0.8	0.5	0.4
Line Width Roughness (nm) <8% of CD	3.0	2.0	1.4	1.0	0.7	0.6
Precision for LWR	0.6	0.4	0.3	0.2	0.1	0.1
Overlay Control (nm) (mean +3σ)	32.0	23	16	11	7	
Overlay Metrology Precision (nm) P/T=0.1	3.2	2.3	1.6	1.1	0.7	

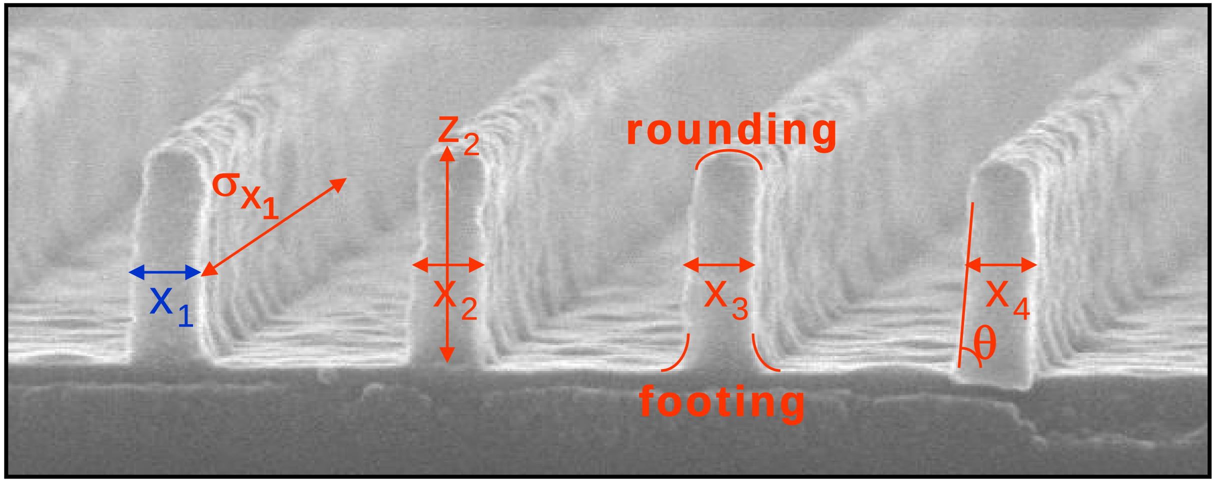
ITRS does not tell the whole story…

- ITRS is focused on precision, but there are other pattern metrology development needs
  - Reliable pattern height and sidewall metrology to monitor shrinking process windows
  - Overlay targets that accurately reflect in-chip registration
  - Accurate and traceable 3-D reference metrology
  - Design-based metrology (DBM) to support RET
  - Robust integrated metrology with proven ROI
- Metrology problems are complicated by APC requirements
  - APC reduces process variance beyond ITRS specifications, so the metrology precision must scale accordingly
  - APC can not distinguish between process and metrology trends, so metrology stability is critical

Pattern Fidelity Metrology

- For 90-nm and beyond, it is not enough to know the width of a single printed line
- Robust litho metrology must be able to answer the question:

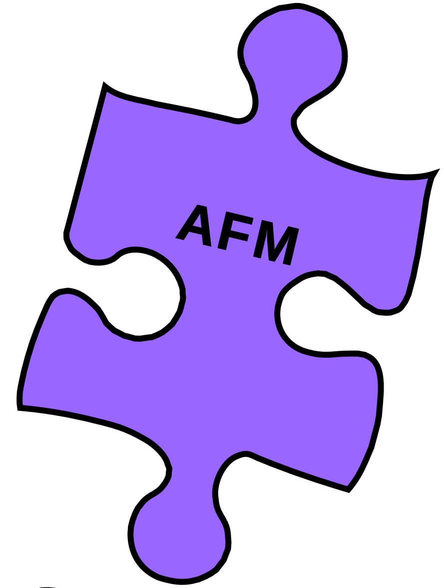
  "How accurately did I reproduce the mask pattern in all three dimensions?"
- **Old Paradigm:** What is the CD of this array?
  - Metrology: point solution CD (X_1)
- **Beyond 90-nm:** What is the **pattern fidelity** of this array?
  - Metrology: 3-dimensional details (X_{1-4}, X_{bar}, σ_x, θ, Z, footing, rounding)

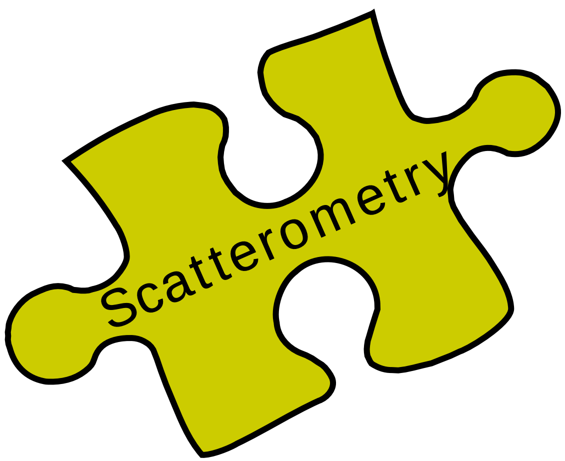


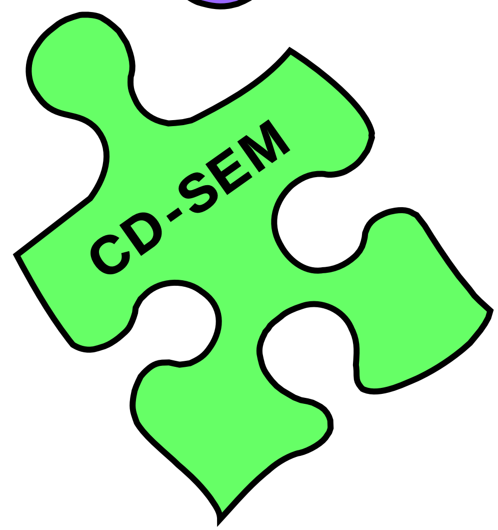
Cross-section SEM image of 90-nm gate resist lines.

Pattern Fidelity Metrology

- What are the capabilities of each technology?
- What is the right mix to satisfy my control needs and maximize ROI?





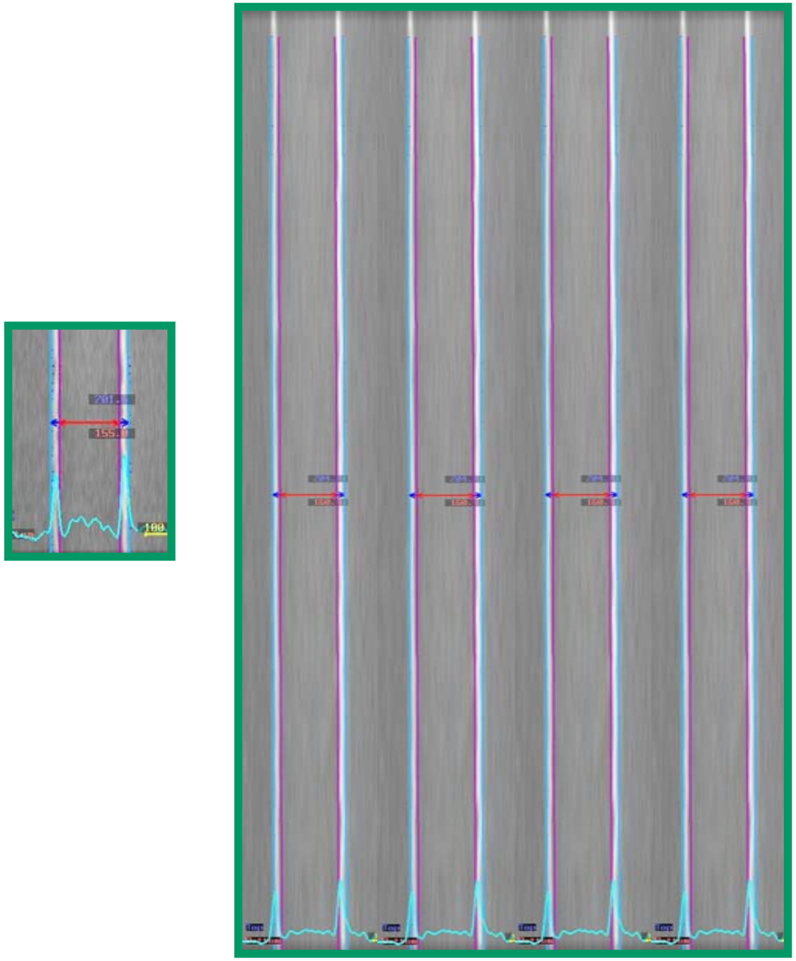


CD-SEM

- Strengths
  - Measurement flexibility
    - *Logic ring oscillator*
    - *Flash core array*
    - *Special test or electrical structures*
    - *OPC validation features*
  - Localized statistics
  - Line roughness
  - Low overhead, low risk
    - *Short setup time*
    - *No modeling constraints*
    - *Proven technology*
    - *Proven automation*

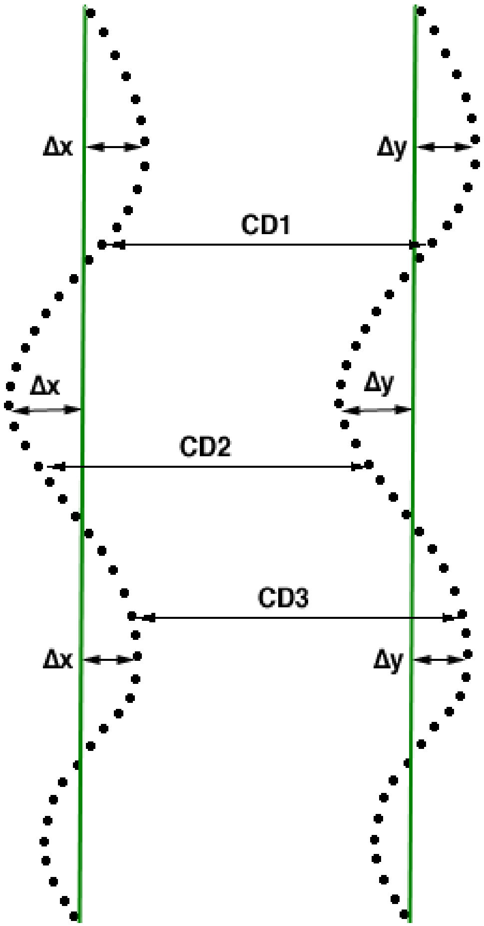
Advanced CD-SEM Measurements

- Advances in SEM column design and measurement algorithms have enabled much larger measurement areas
- Benefits:
  - Up to 100x more signal averaging
    - *Better tool precision and correlation to device*
  - More accurate roughness measurements
    - *Larger sample eliminates short range bias*
  - Local CD variation analysis
    - *Determine line-to-line CD errors*



Old (left) vs. New CD-SEM Measurement Region

CD-SEM Line Roughness



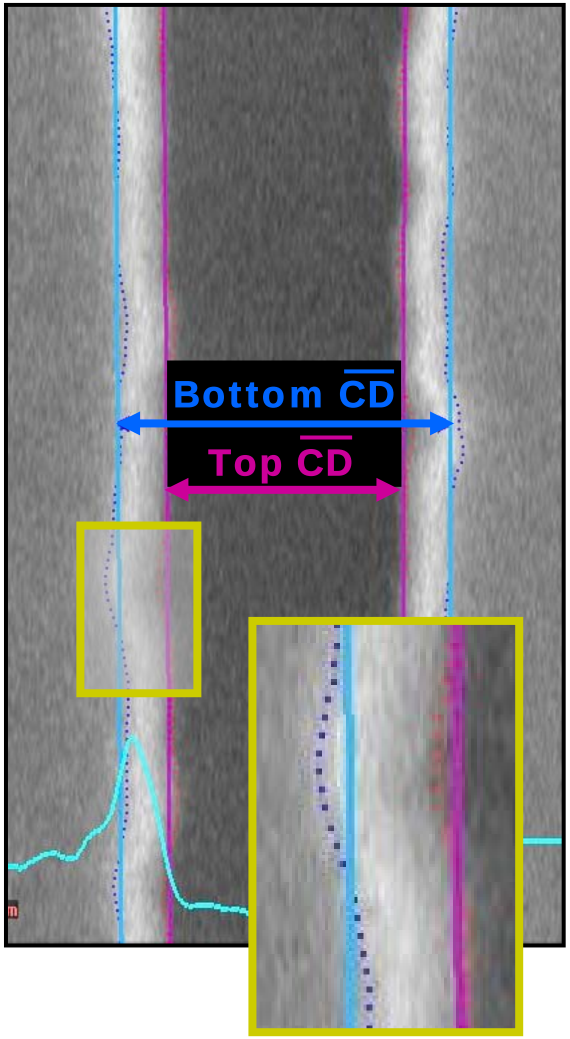
Line Width Roughness (LWR)

$$LWR = 3\sqrt{\frac{\sum_i (CD_i - \overline{CD})^2}{n-1}}$$

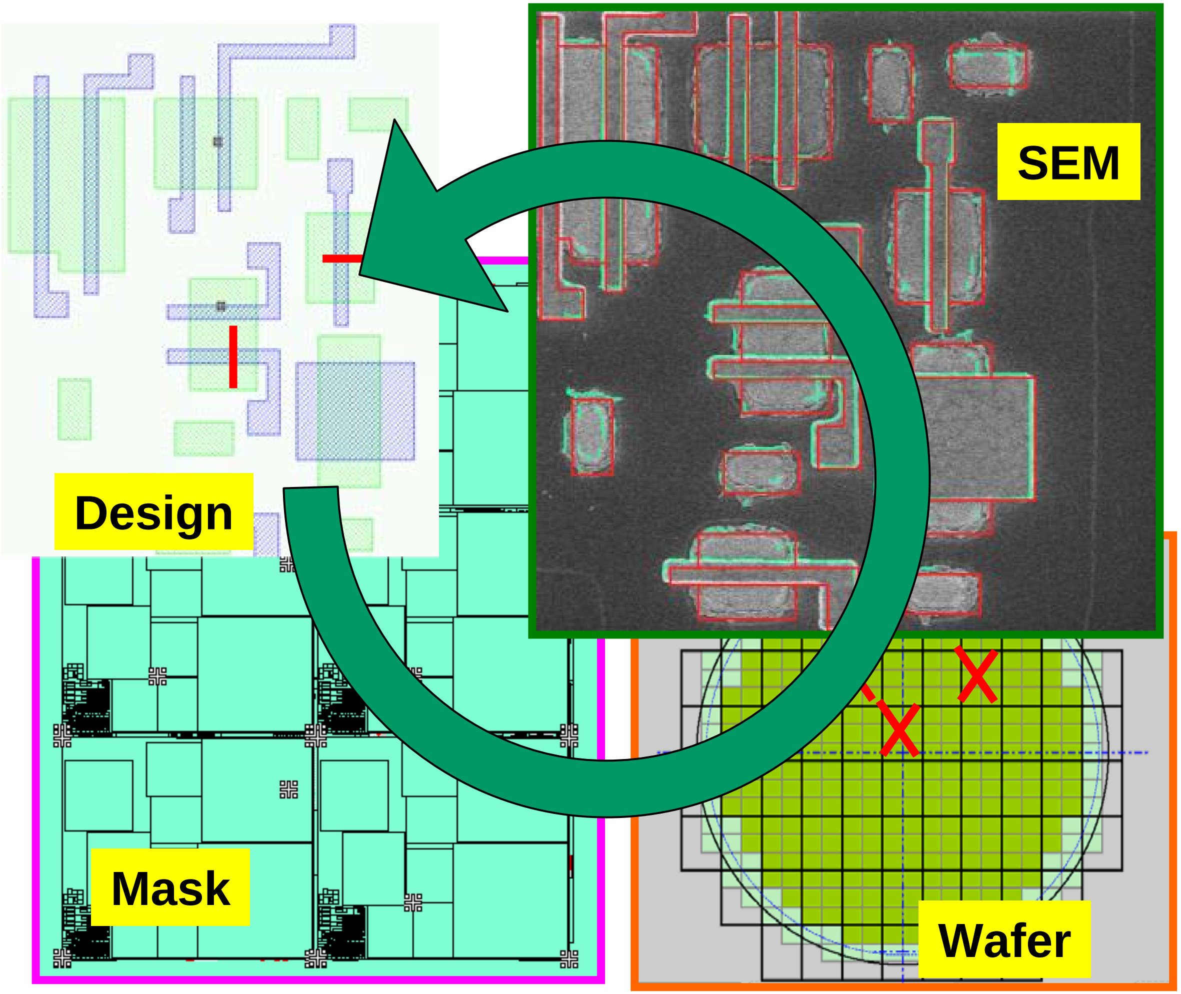
Line Edge Roughness (LER)

$$LER_x = 3\sqrt{\frac{\sum(\Delta x)^2}{n-1}}x$$

- Line edge roughness alone can swamp the entire projected CD budget
- CD-SEM roughness measurement capabilities are steadily improving



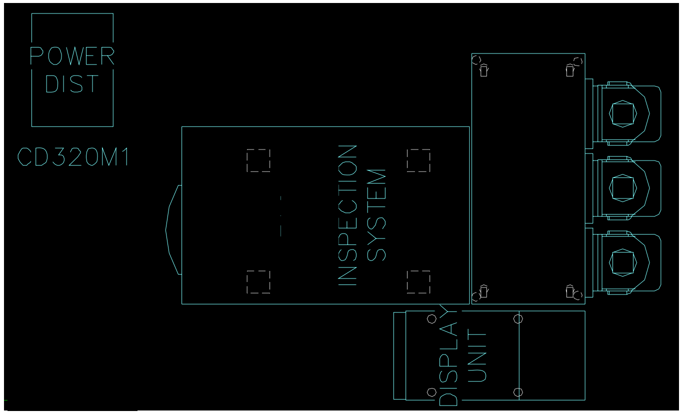
Design-Based Metrology (DBM)



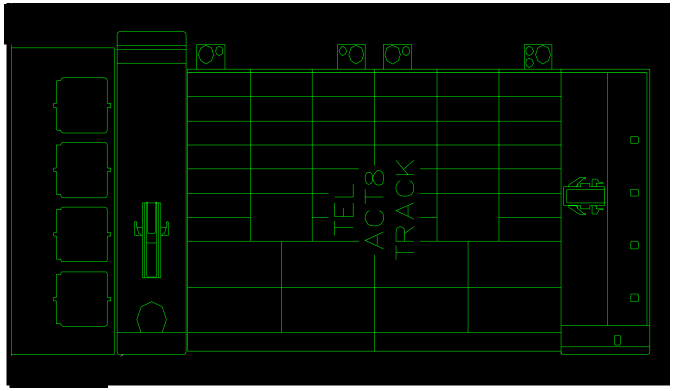
- Shrinking pitch and CD targets cause large proximity effects
- Optical Proximity Corrections (OPC) are designed into the mask to make the wafer image match design intent
- OPC model building and validation requires thousands of wafer measurements
- AMD has helped pioneer the creation of SEM recipes automatically from design data
- The SEM will soon be able to score the agreement between wafer and design

CD-SEM Weaknesses

- Large Size
  - No integration
  - **Growing footprint**
- Price per unit
  - Advanced tools list at $2-3M
- Throughput (MAM ~3.5 sec)
  - Better than AFM
  - Worse than scatterometry
- Capability constraints
  - Limited 3-D metrology
  - Voltage vs. S/N constraints
- High uncertainty
  - Inadequate calibration standards
- Sample interaction
  - 193-nm resist shrinkage

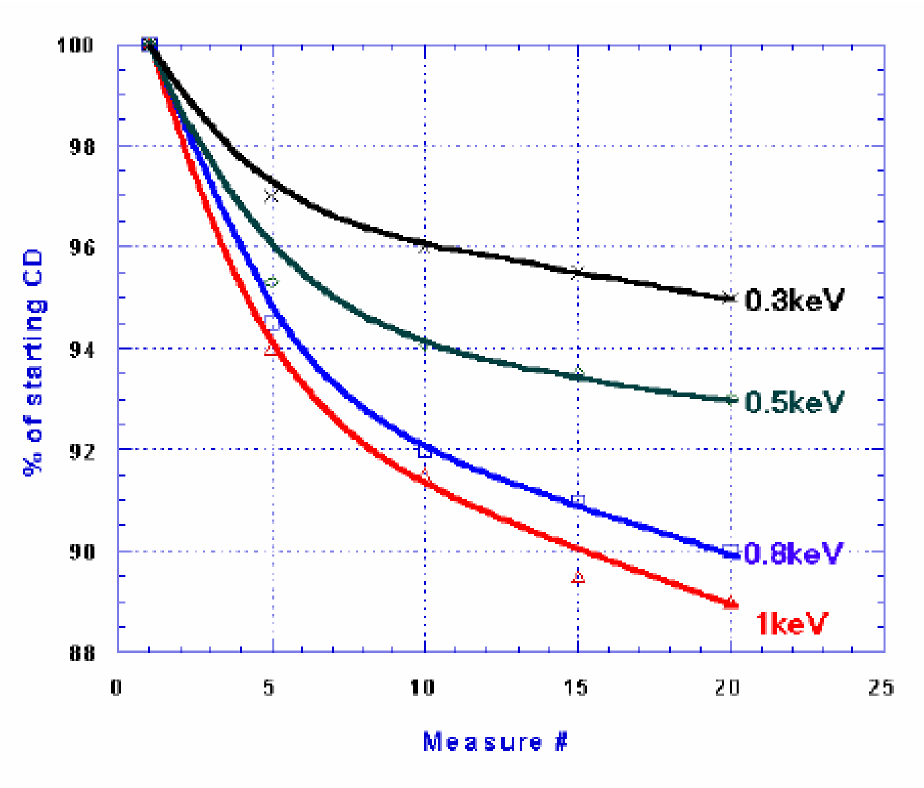


CAD Icon for New CD-SEM



CAD Icon for New Track

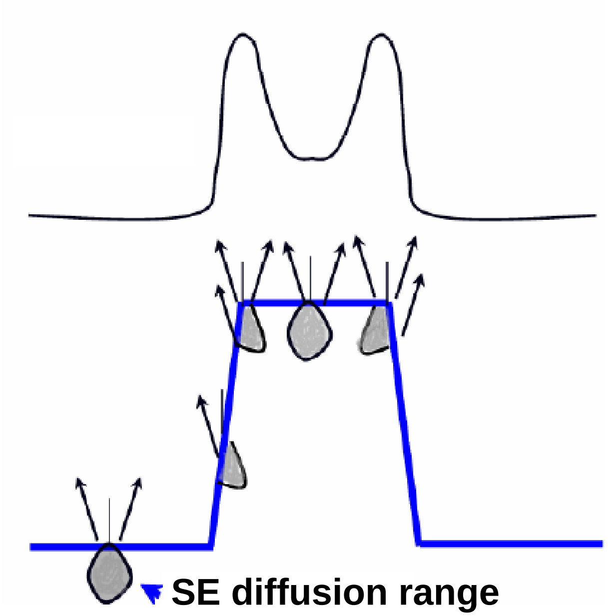
193-nm Resist Shrinkage

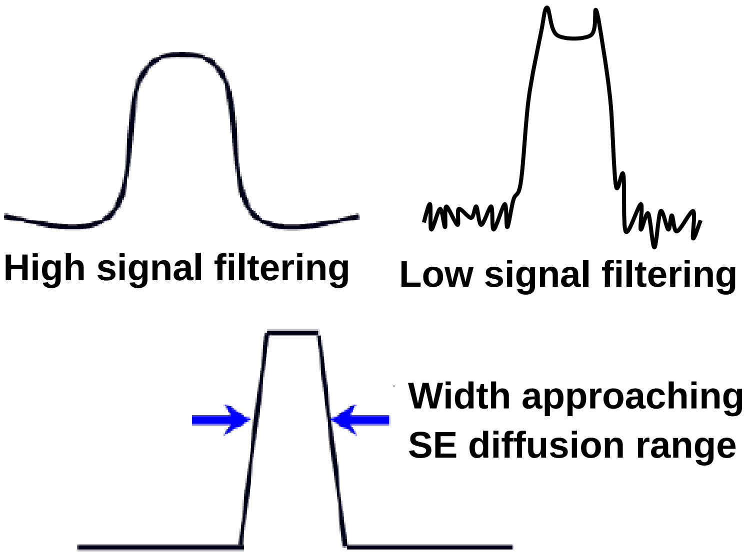


- Resist shrinkage issues are driving CD-SEM manufacturers to lower accelerating voltages
- But these lower voltages cause severe electron-optic problems
  - Fewer secondary electrons cause lower S/N per scan
  - Reduces precision
- To mitigate the problem
  - Use more scans per measurement (higher sampling)
  - Use larger waveform filters

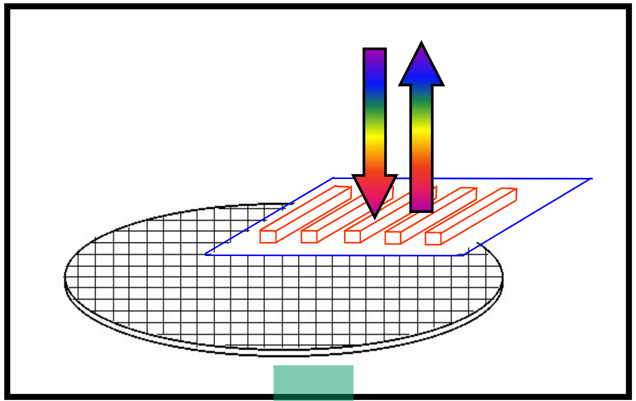
The Edge Detection Problem

- Most CD-SEM algorithms use peaks from a secondary electron (SE) intensity curve to find feature edges
- Gate lines at the 45-nm node will be near the SE diffusion range, limiting the ability to separate edges
- Competing objectives:
  - Lower energy requires higher filtering to overcome S/N issues
  - Smaller lines require smaller filters to distinguish edges

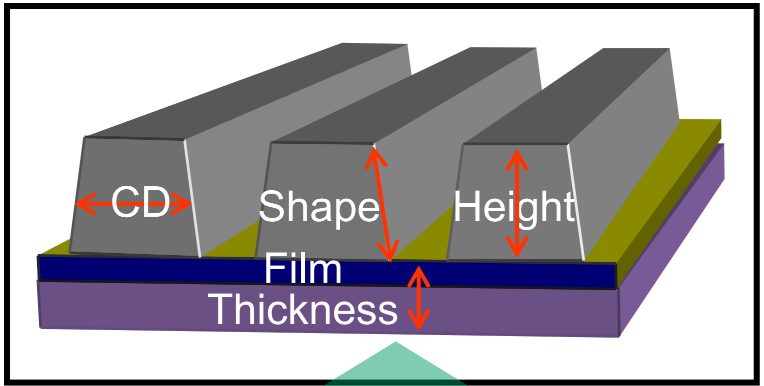




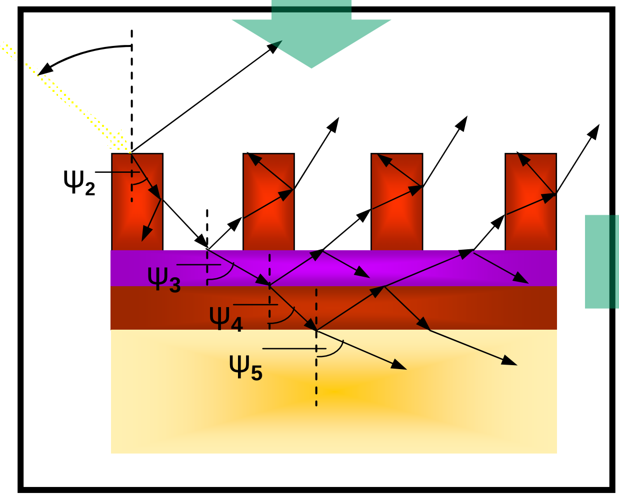
Scatterometry Overview



Broadband Light is directed at a grating

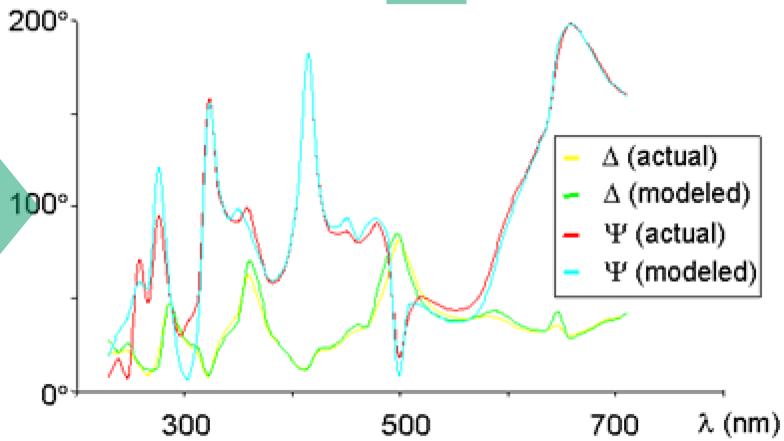


Model Parameters are Output



The light interacts with the sample

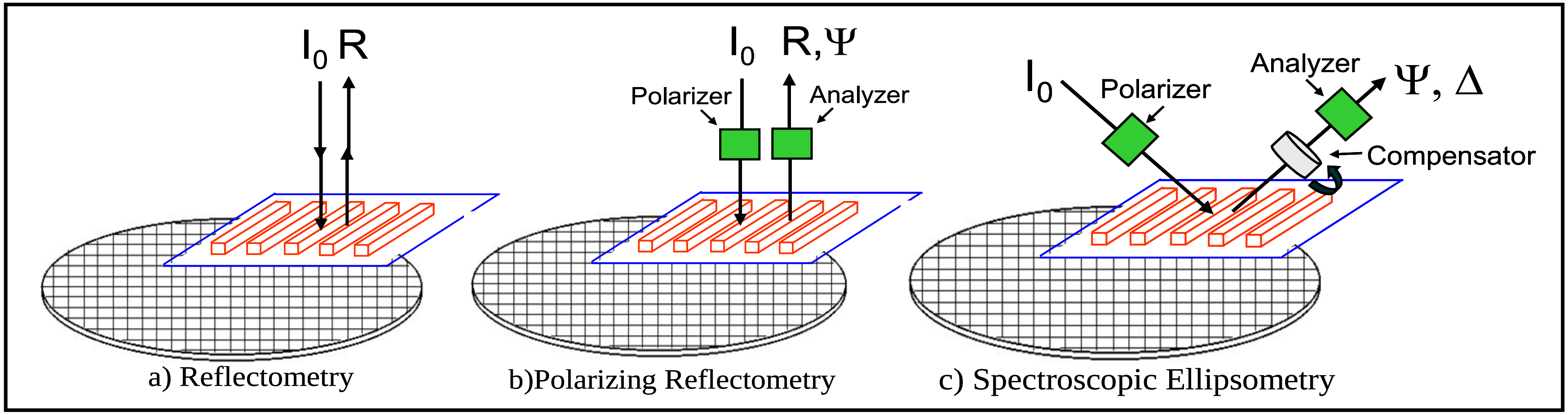
Regression or Library



Signature is Matched to Theoretical Solution

AMD

Broadband Scatterometry Hardware



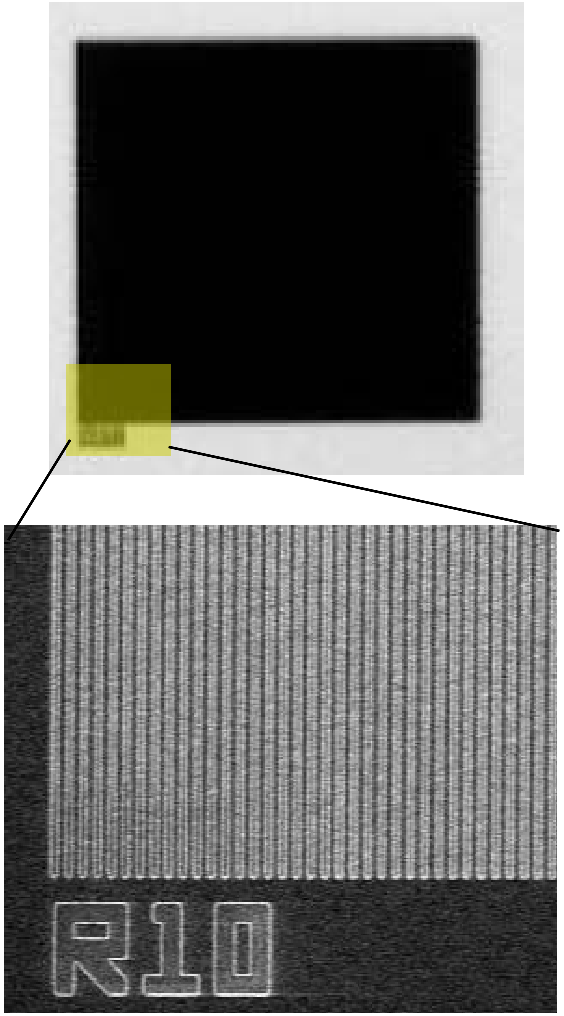
a) Spectroscopic Reflectometry (R)
- Normal incidence and relatively simple optics (small, fast, cheap)
- Worst sensitivity and accuracy
- Best signal to noise

b) Polarizing Reflectometry (Rp)
- Normal incidence with polarizing optics
- Small, but not as fast or cheap as simple reflectometry
- Improved sensitivity and accuracy, but not SE quality

c) Spectroscopic Ellipsometry (SE)
- Oblique incidence with polarizing and rotating elements
- Best sensitivity and accuracy (phase and intensity response)
- Large tool, large spot size, high cost

Scatterometry Strengths

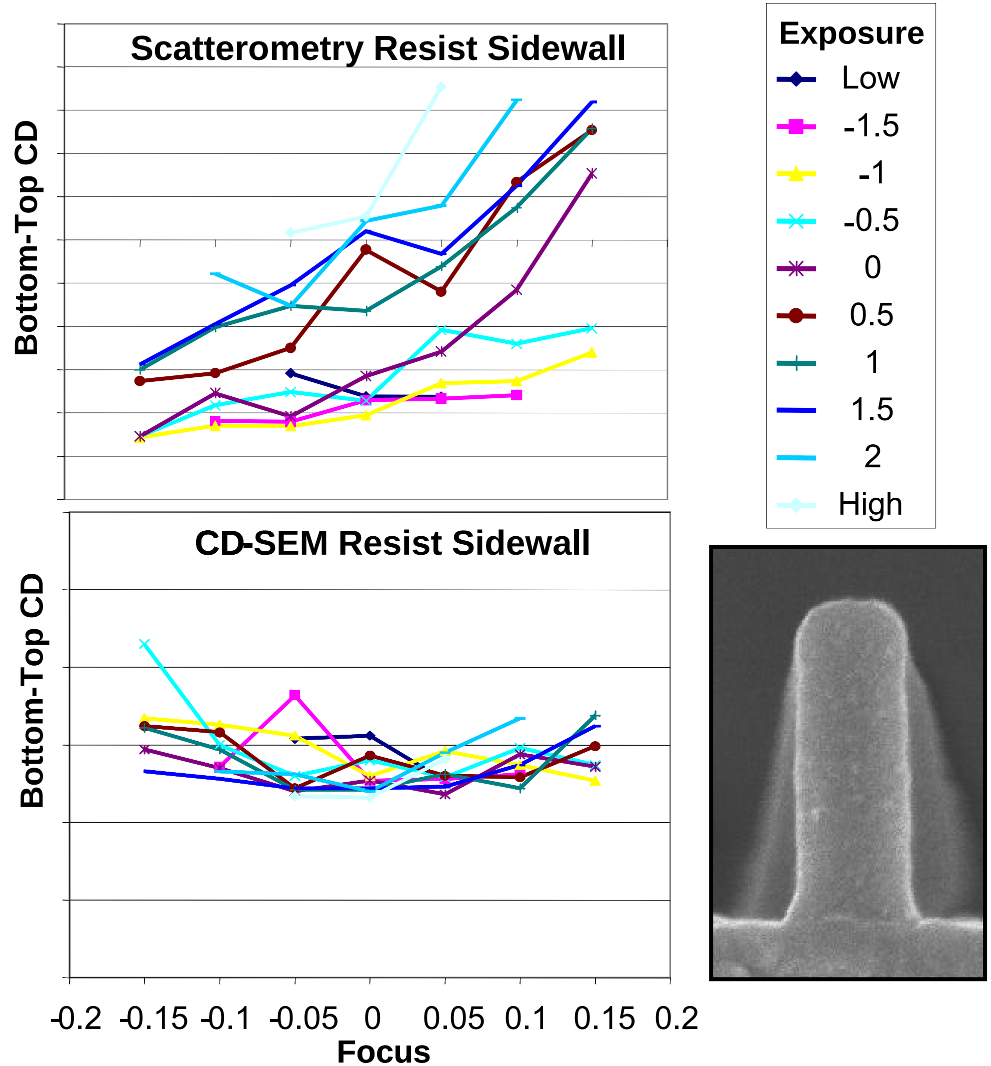
- Rich data stream
  - Profile information
  - Feature height
  - Underlying film thicknesses
- High degree of signal averaging
  - Sample spectra is essentially an average of hundreds of lines in the diffraction array
  - Good precision
  - No localized CD effects
- Suitable for process tool integration
  - Small size and high throughput
  - Selecting hardware is a function of requirements



Optical and SEM grating images

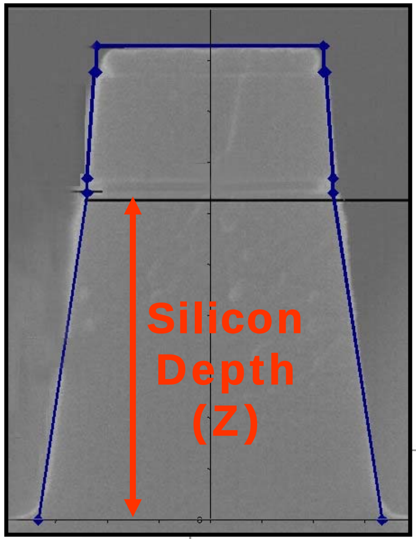
Resist Profile Metrology

- Scatterometry is capable of returning the sidewall angle of the feature
- The CD-SEM is incapable of measuring sidewall variation, especially for vertical or reentrant profiles
- Shrinking process windows make it critical to separate dose and defocus errors
- Current paradigm: Exposure control using CD-SEM
- 65-nm and beyond: Simultaneous exposure and focus control using scatterometry

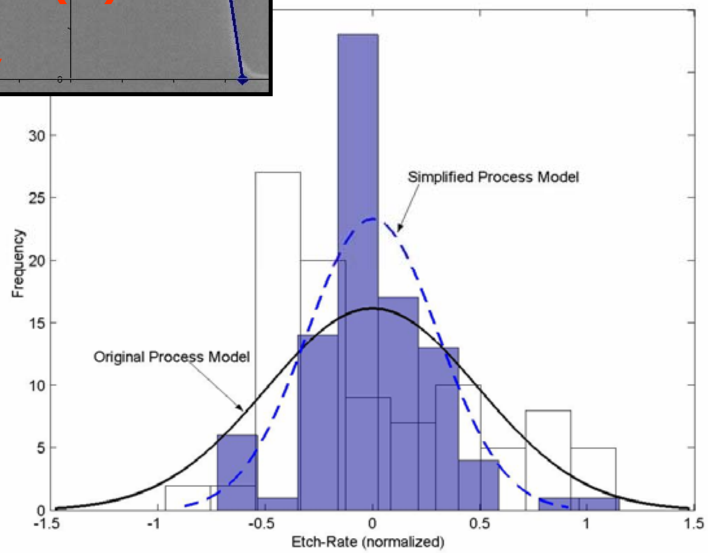


Feature Height Metrology

- STI etch depth metrology migrated from the profilometer to scatterometry
- Benefits:
  - Simplified APC model by allowing direct measurements of features that previously had to be derived.
  - Increased capacity by implementing a faster metrology technology and eliminating some metrology operations.
  - Reduced Cost by eliminating the need multiple metrology types for profile, thickness, and CD measurements.
  - **Improved process control** due to improved metrology precision



Cpk improvement of 90% for STI Etch RtR by adopting Scatterometry.

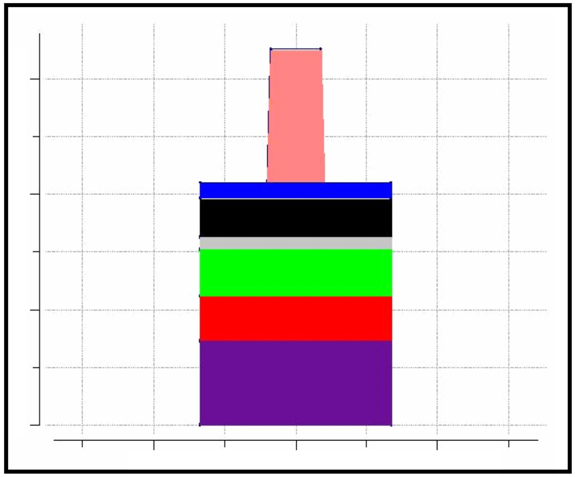


Scatterometry Weaknesses

- Feasibility is determined per application
  - Depends on film stack, grating layout, and hardware used
  - Advanced anti-reflective coatings limit reflectance
  - Small features are driving spectral response to lower wavelengths
  - Rich data streams quickly become poor
- High overhead
  - Significant expertise required to develop and test models
  - Spectroscopic n&k must be generated for every film
  - Library building is time consuming and real-time results are unreliable
  - Grating structures must be designed into reticles
- Hardware tradeoffs
  - Fast, cheap and stable, vs. slow, expensive, and sensitive
  - The right choice may vary for IM vs. stand-alone applications
  - Mix and match, or compromise?
- Fundamental capability limitations
  - No roughness data, contact holes still unproven
  - Measurements restricted to large scribe-line test structures
  - Sensitivity decreases from dense to isolated features

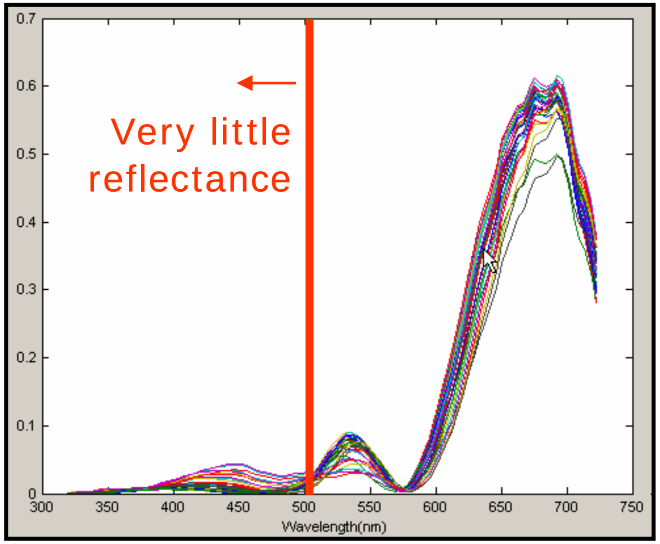
The ARC Problem

- Scatterometry and ARCs are diametrically opposed
  - Scatterometry requires reflectance
  - ARC stands for Anti-Reflective Coating
- ARC films can limit scatterometry sensitivity
  - Simplified models are required
  - Fixed film thicknesses and diminished profile information



90-nm Gate stack

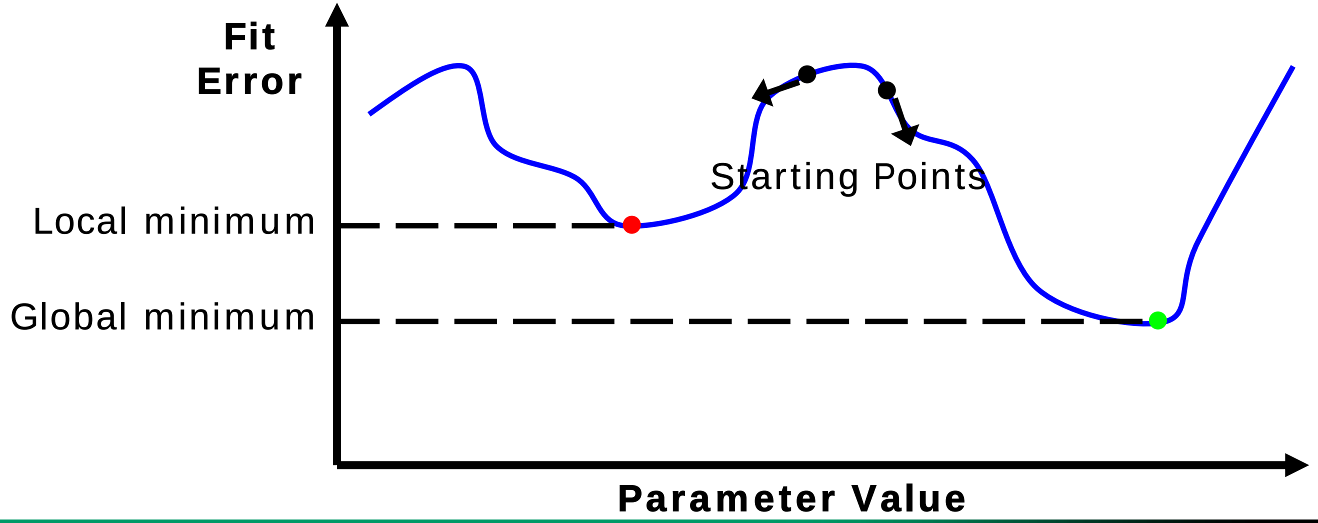
90-nm Gate Application
- 7 underlying blanket films
- Organic ARC
- 1:3 line to space ratio
- Little signal below 500-nm
- Resist must be modeled as rectangle



Reflectance spectra from FEM wafer

The Regression Problem

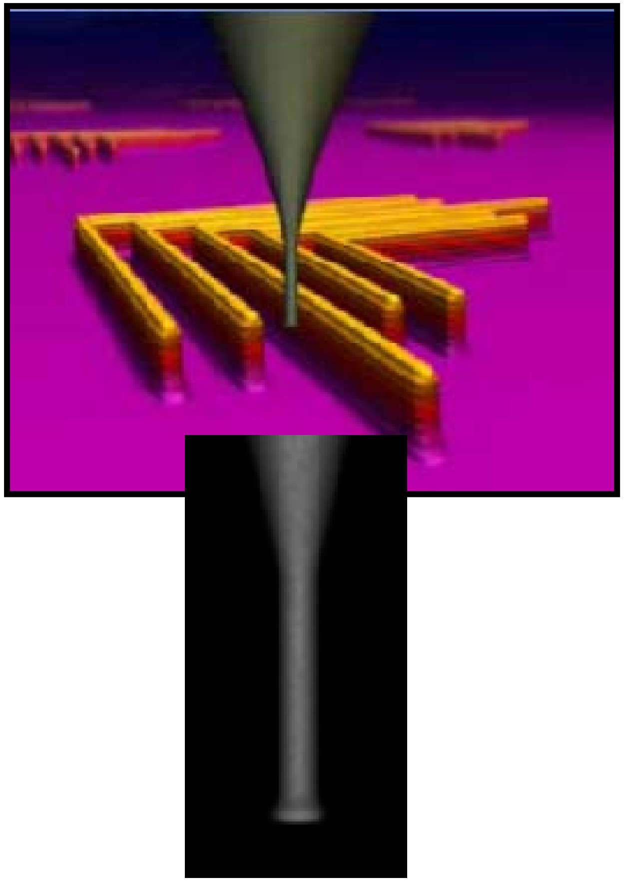
- Scatterometry Libraries
  - Nearly instantaneous, guaranteed “global” best match
  - But library generation is time consuming
  - And process changes may require a new library
- Regression or “real-time” approaches
  - Does not require library build
  - Match is slower, especially for complex models
  - Sensitive to initial position, may be trapped in local minima
- Some suppliers are working on “hybrid” approaches



Atomic Force Microscopy (AFM)

- AFM is a mature technology for step height and analytical metrology
  - Extremely accurate in X and Z dimensions
  - Also very slow and engineering intensive

- AFM improvements are driving fab implementation for pattern metrology
  - Throughput and automation capabilities are being improved
  - Tips are becoming smaller to match shrinking geometries (carbon nanotubes)
  - Flared tips are being used to image feature sidewalls

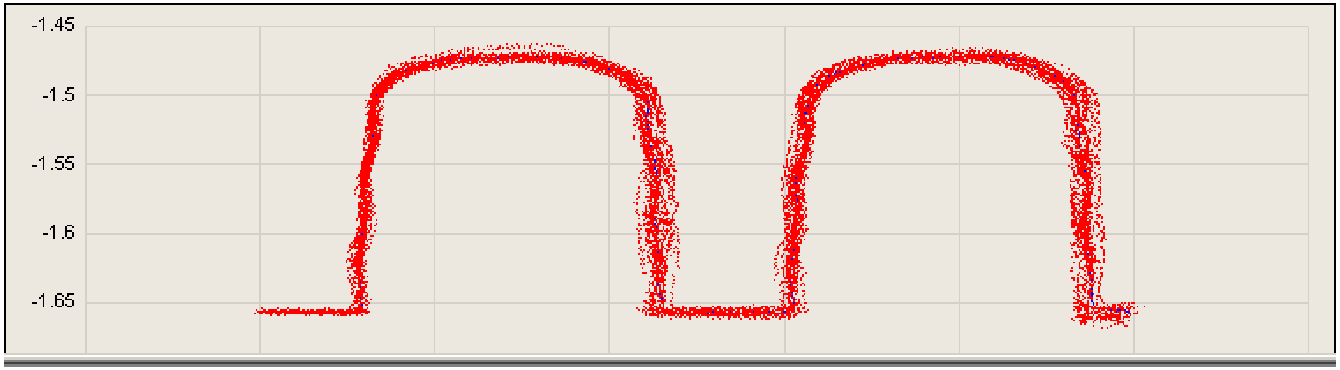


Flared AFM tips enable sidewall imaging

Graphics from Veeco Dimension X3D™ promotional material

AFM Applications

- AFM is a complimentary technology
  - AFM is too slow and engineering intensive to use for large-volume process control
  - Instead it will support CD-SEM and scatterometry as a powerful reference tool
    - *Validate profile information from scatterometry*
    - *Calibrate CD-SEM and scatterometry metrics*
    - *Supply profile information for litho cell quals where scatterometry applications are not feasible*
    - *Reduce requirement for destructive cross-section SEM analysis*



Veeco Dimension X3D resist profile data

Integrated Pattern Fidelity Metrology

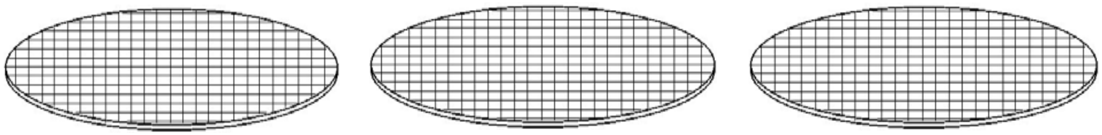
- IM tools based on scatterometry are commercially available
- Litho Track IM
  - Must be small, fast and stable (R or Rp?)
  - Reflectometers have sensitivity issues
  - How do we meet productivity and technical requirements?
- Etch IM
  - Throughput and size constraints not as severe (SE?)
  - Must be resistant to corrosive gases
  - Complex modeling challenges, including polymer layer
- Compatibility with stand-alone
  - Ideally there would be one platform for all three applications
  - But can one platform meet all requirements?
- Business constraints
  - Metrology and process tool vendors have restricted agreements
  - If a customer can develop a comprehensive strategy, can it be delivered?

AMD

IM and Wafer-Level Control

Wafer Level Control (all information supplied prior to processing)

Specify recipe parameters for each wafer → Process Wafer #1 → Process Wafer #2 → Process Wafer #3 → etc



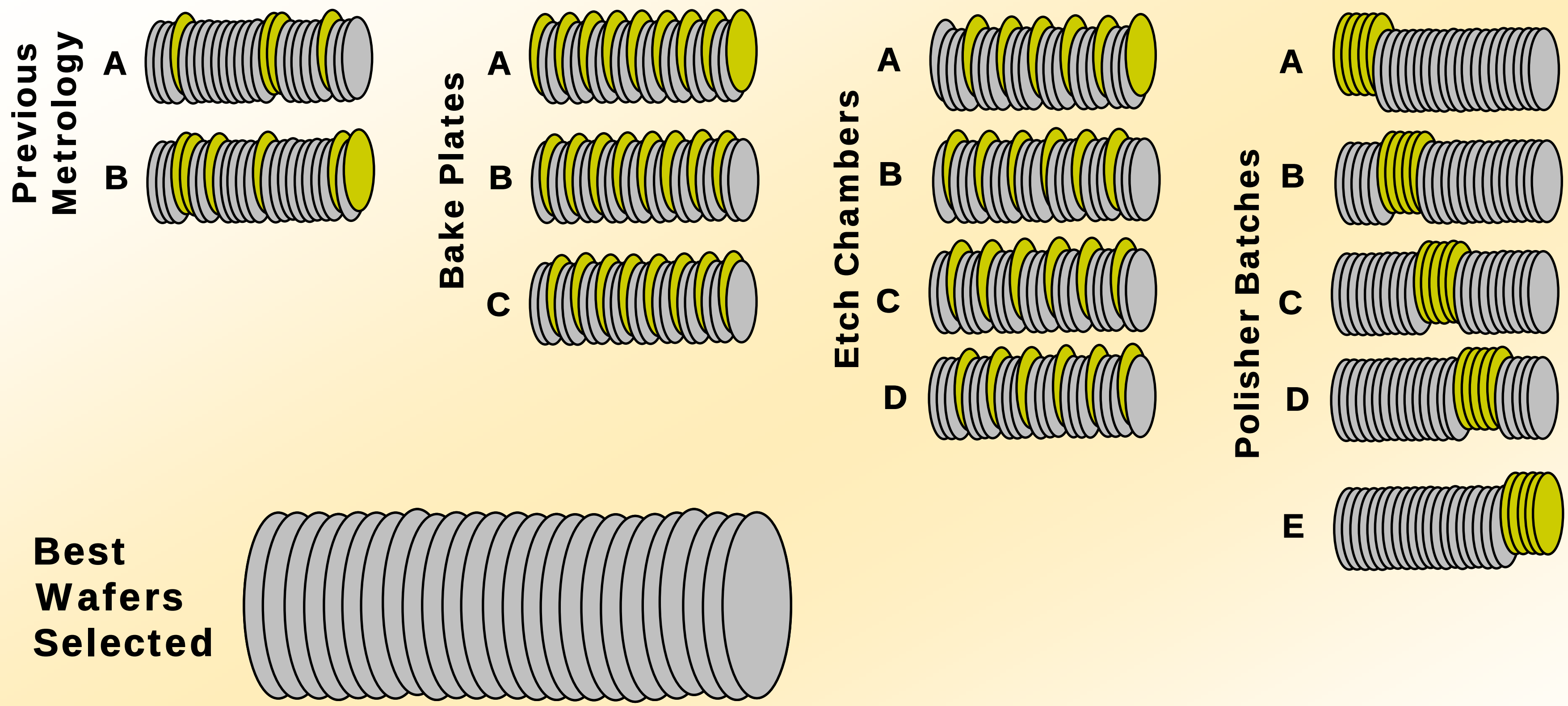
Wafer-to-Wafer Control (requires new information during processing)

Adjust recipe parameters for Wafer #1 → Process Wafer #1 → Adjust recipe parameters for Wafer #2 → Process Wafer #2 → etc

- Integrated Metrology is required for wafer-to-wafer control, but not wafer level control
- *How does AMD do WLC without IM?*

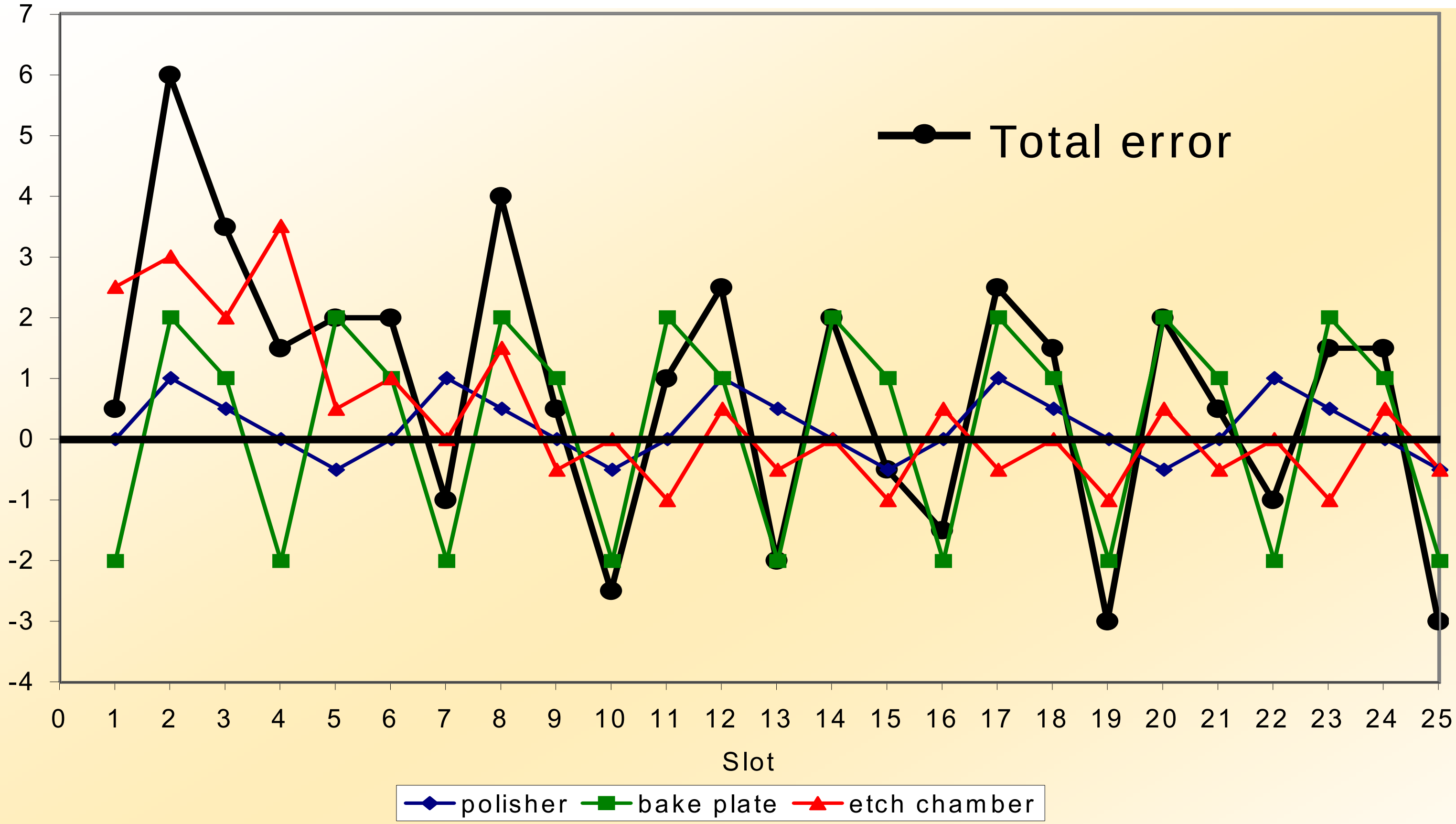
AMD

Dynamic Wafer Level Sampling



- Utilizes wafer processing history to determine which wafers provide the most valuable information.
- Over time, all sources of variation or characterized

Within-Lot Sources of Variation

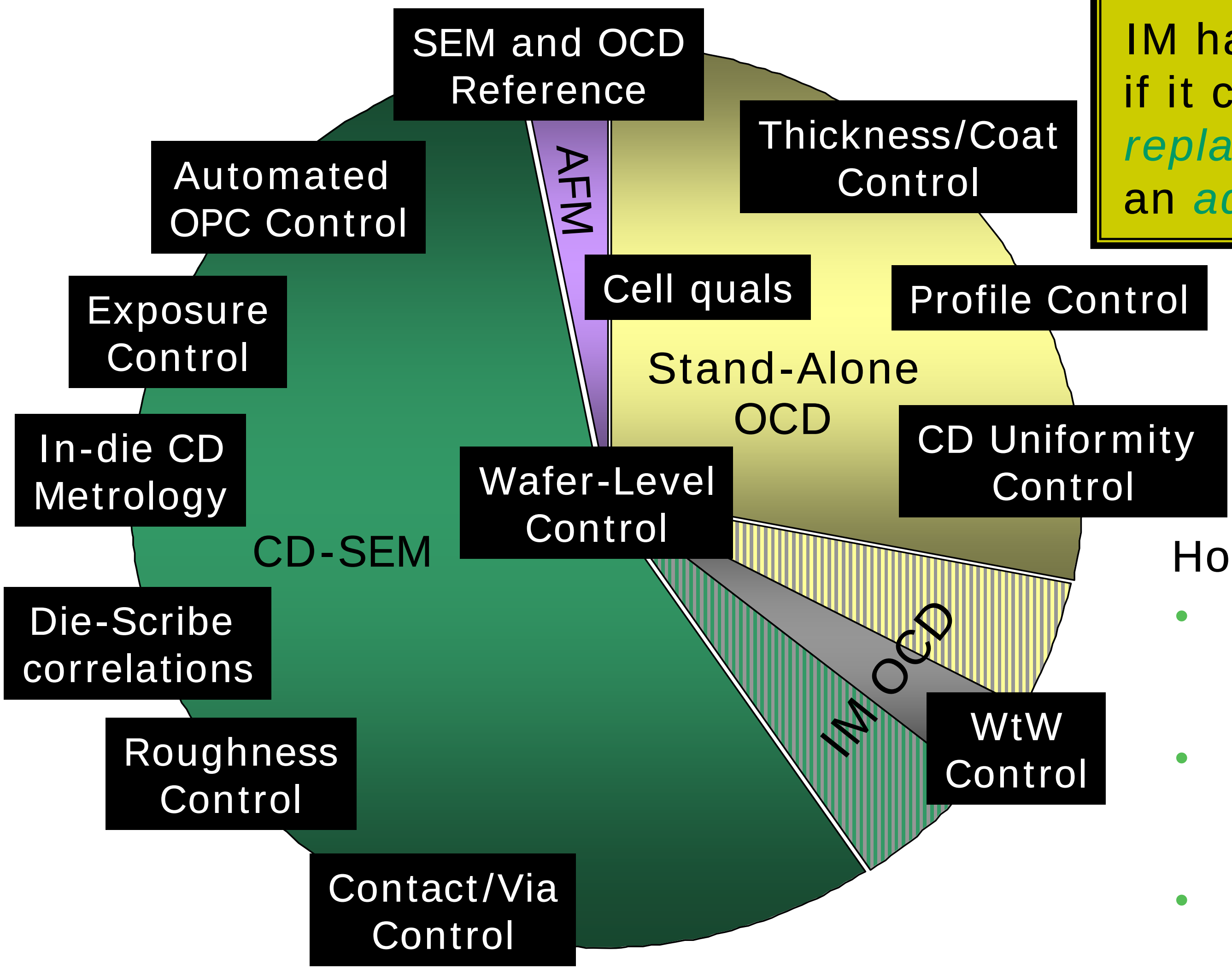


- Within wafer variability is largely made up of semi-static contributions
- Our wafer-level control scheme corrects for this variability
- Pure wafer-to-wafer control would actually be ineffective

Integrated Metrology Drivers

- Control requirements
  - Most wafer-level control can be done with stand-alone tools
  - Wafer-to-wafer control only needed for critical steps with small process windows and high transient variability
  - At those critical steps, sensitivity to parameters of interest is in doubt
- Operational Efficiency
  - Streamlined factory automation
  - Eliminate metrology steps
  - Reduced cycle time
- Cost-of-ownership
  - Reduced floor space requirements
  - Reduced capital required for stand-alone metrology

Pattern Fidelity Metrology Mix



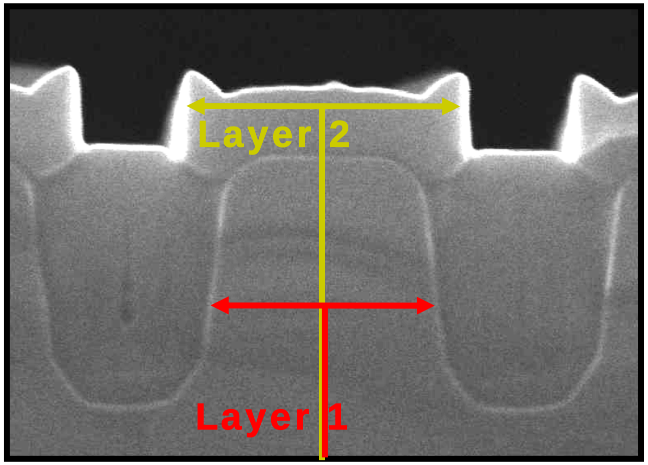
IM has significant upside if it can become a *replacement* rather than an *additional* technology.

How?

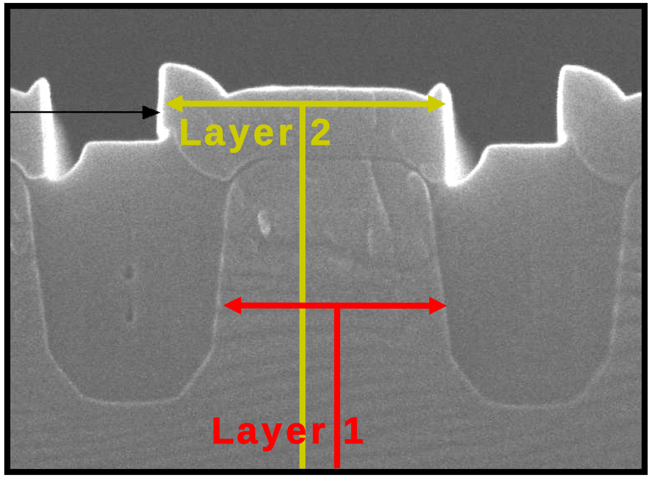
- Systematically address technology weaknesses
- Create a marketable fab-wide hardware strategy
- Drive down CoO to match stand-alone model

Pattern Placement Metrology

- According to the ITRS, overlay should be fine...
  - Precision requirements down to 45-nm can be met with the current toolsets
  - 32-nm precision looks achievable with minor changes
- But what about Overlay Mark Fidelity (OMF)?
  - OMF refers to the degree to which overlay test structures accurately predict in-chip registration



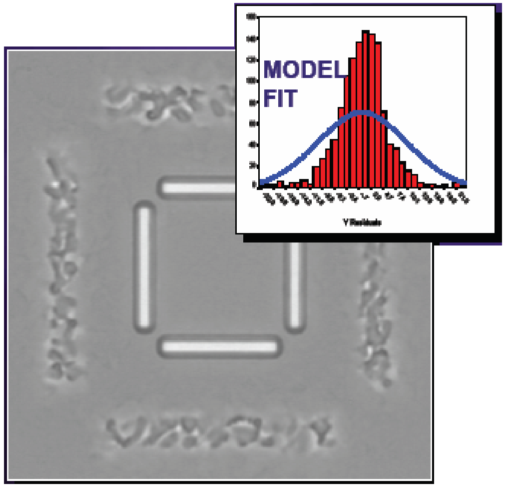
Good In-chip Registration



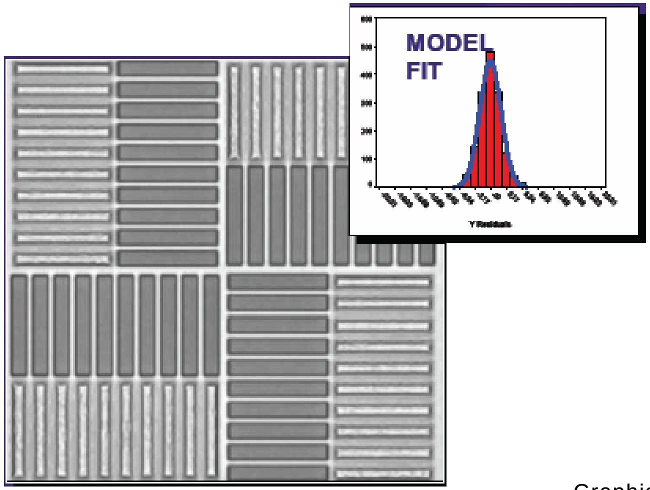
Poor In-chip Registration

Overlay Mark Fidelity (OMF)

- Traditional box-in-box overlay marks are showing poor OMF at the 65-nm node
  - Scribe-line test structures fail to model across-chip variation
  - Large test patterns show different scanner/lens induced placement error than design-rule device features
- Grating-based targets show improved OMF, driving down model residuals and improving APC performance



Box-in-box Target

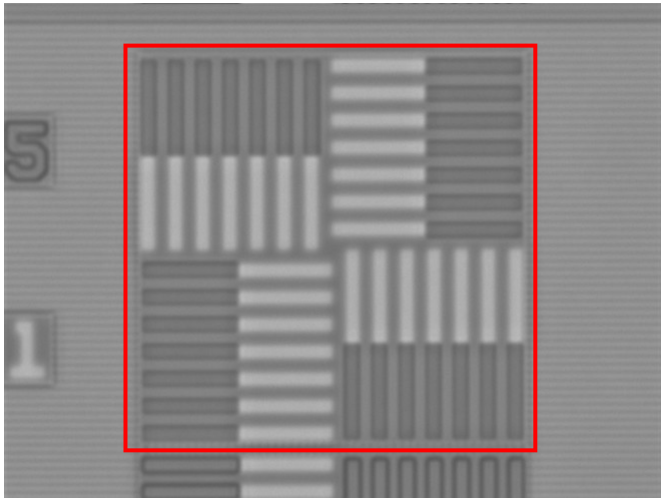


Grating Target

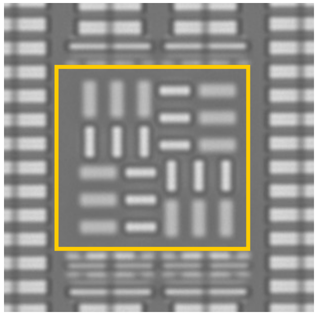
Graphics from "Microeconomics of Overlay Control at the 65-nm Node," Algair and Monahan, ISSM 2003

In-Chip Overlay Targets

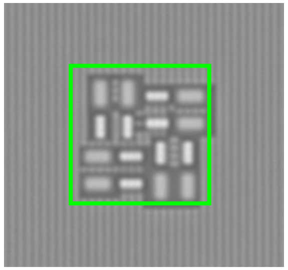
- Even if scribe-line structures show *perfect* OMF, it is still impossible to model some error sources that are non-linear across the field
- Smaller targets must be developed that can be dropped into the device for better in-chip measurements
- *To adequately support the industry, target designs must not be proprietary!*



Standard 30x30um Grating



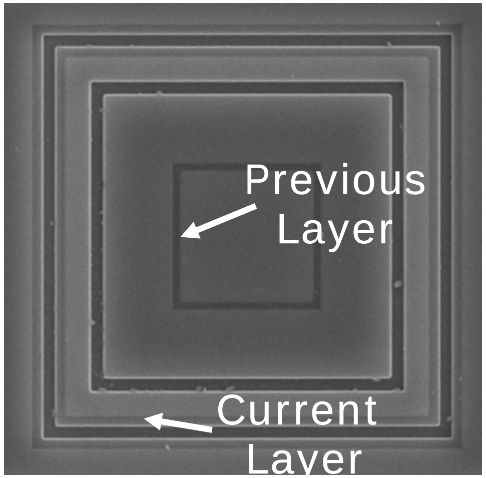
3-finger 13x13um μTarget



2-finger 11x11um μTarget

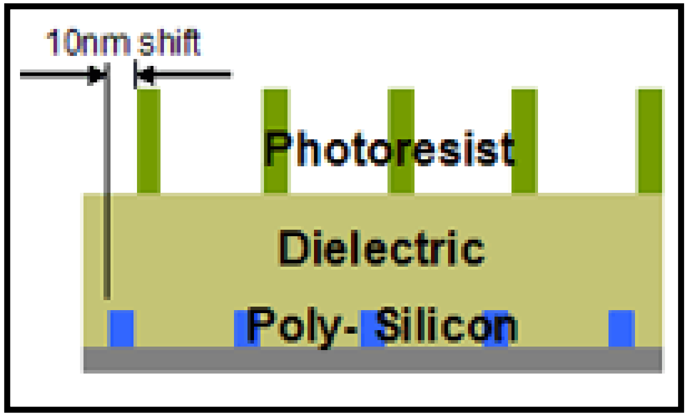
Emerging Pattern Placement Metrology

- SEM
  - At high voltages, SEM tools can image previous layer structures
  - Promises good precision and OMF



20keV SEM image of overlay target

- Diffraction
  - Model the diffraction signal from overlapping structures
  - Similar to scatterometry

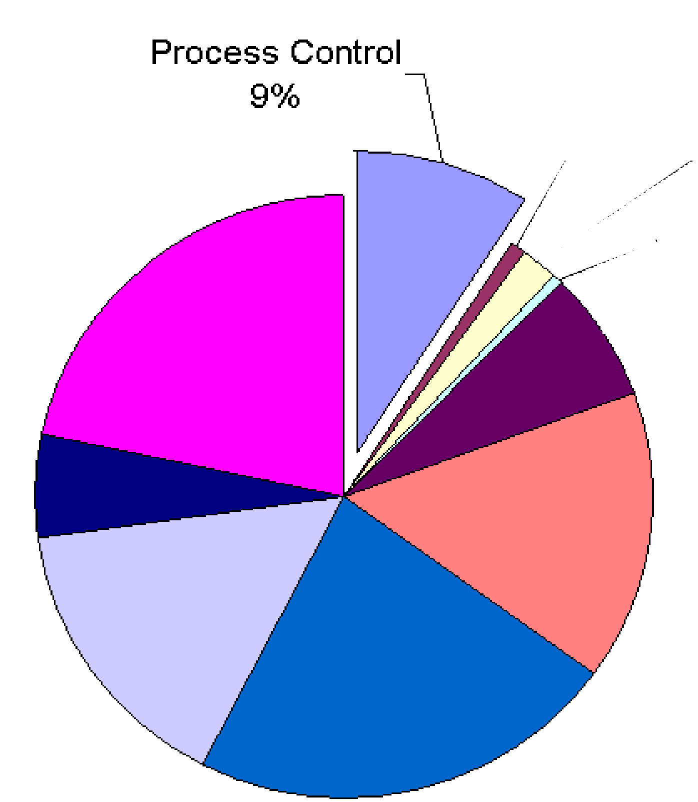


Schematic of diffraction overlay target

Integrated Overlay Metrology

- Multiple overlay vendors are actively developing integrated metrology units
- Operational efficiency, rather than control requirements, will be the primary driver for overlay IM
  - Litho cells are the bottleneck tools for modern fabs
  - Metrology delay and sparse sampling cause APC-induced idle time
  - IM would eliminate idle time due to sparse metrology

Up to 9% of idle time on a litho cell can be the result of process control business logic.



Causes of Stepper Idle Time

Pattern Placement Summary

- What makes up the true overlay error budget and how do we measure it?
  - New optical target designs are improving OMF
  - Paradigm-shifting technologies are in their infancy
  - What technology will be the AFM of the pattern placement arena?
- Overlay metrology right now is similar to CD metrology 5-10 years ago
  - We are just starting understand challenges and evaluate alternatives
  - People will make false generalizations about the future of optical overlay
  - The most likely scenario is that optical overlay will evolve and new technologies will gain traction in critical areas
- Integrated metrology for overlay has a place
  - Like pattern fidelity IM, the ROI is the hardest part
  - Metrology vendors must work closely with their customers

Dual-Core AMD Opteron™ Processor
The Manufacturing Challenge Continues

90nm Process

Approximately same die size as 130nm single-core AMD Opteron™ processor*

~205 million transistors*

95 Watt Power Envelope

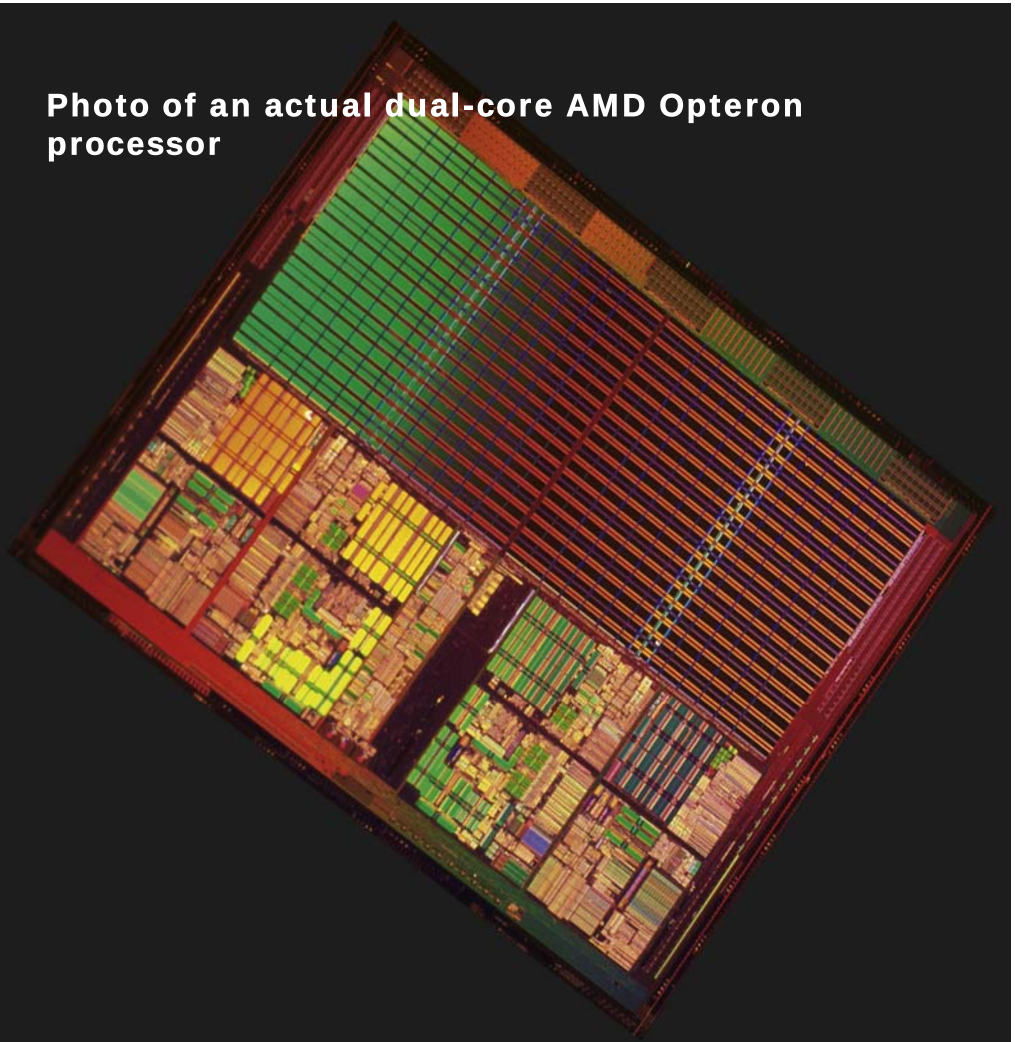
Fits into 90nm power infrastructure

Only requirement is a BIOS upgrade

Requires Strong Yields on Large Die

Enabled by F30's highly successful 90nm transition

Photo of an actual dual-core AMD Opteron processor



*Based on current revisions of the design

AMD Fab 36: AMD's Latest Benchmark Fab

Expected to be the most advanced 300mm fab in the world

First test wafer starts in April 2005

Only 16 months from ground breaking to first silicon
On track for volume production in 2006

Planned for 65nm, 45nm and 32nm technology generations

Trends & Conclusions

- Pattern metrology is not easy!
  - A comprehensive control strategy for 65-nm requires a complex mix of tools
  - Many of the solutions that the industry is relying upon for 65-nm will be immature and engineering intensive
  - Pervasive APC adds an extra layer of requirements relative to previous technology nodes
- The case for IM is a work in progress
  - Technology and cost constraints have forced AMD to develop wafer-level control strategies that do not require IM
  - Slow progress has created a high activation energy

    Technology risk is still too high to bet the fab on

    IM must become a replacement technology
  - **But the upside is there if we continue to eliminate cost and technology barriers!**

AMD

Acknowledgments

- Thomas Sonderman
- Matthew Purdy
- Bernd Schultz
- Carsten Hartig
- Craig Sander
- Iraj Emami
- Bhanwar Singh
- Jason Cain
- Sean Hannon
- Ben Bunday (SEMATECH/ISMI)
- David Joy (Oak Ridge National Labs)
- Kevin Monahan (KLA-Tencor)

AMD

Trademark Attribution

- AMD, the AMD Arrow logo and combinations thereof are trademarks of Advanced Micro Devices, Inc. Other product names used in this presentation are for identification purposes only and may be trademarks of their respective companies.